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TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) or 1.97(c))	Docket No. OKI.306

In Re Application Of: **Hideaki MATSUHASHI et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
NEW	FEB. 15, 2002	TO BE ASSIGNED	TO BE ASSIGNED

Title: **METHOD FOR MANUFACTURING FIELD EFFECT TRANSISTOR**

Address to:
Assistant Commissioner for Patents
Washington, D.C. 20231

37 CFR 1.97(b)

1. ☒ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. ☐ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

   ☐ the statement specified in 37 CFR 1.97(e);

   OR

   ☐ the fee set forth in 37 CFR 1.17(p).

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METHOD FOR MANUFACTURING FIELD EFFECT TRANSISTOR

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

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Dated: **FEB. 15, 2002**

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
OKI.306	NEW
Applicant(s)	
Hideaki MATSUHASHI et al.	
Filing Date	**Group Art Unit**
FEB. 15, 2002	TO BE ASSIGNED

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	A	Terukazu Ohno et al., "Experimental 0.25-um-Gate Fully Depleted CMOS/SIMOX Process Using a New Two-Step LOCOS Isolation Technique," IEE Transactions on Electron Devices, Vol. 42, No. 8, August 1995.
	B	T. Naka et al., "A 0.35um Shallow SIMOX/CMOS Technology for Low-Power, High-Speed Applications," The Institute of Electronics, Information and Communication Engineers, Technical Report of IEICE (1997-03), page 45-52.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.